Amendments to the Specification:

Please delete paragraph [0048].

Please replace paragraph [0049] with the following paragraph:

~~FIG. 7~~ FIG. 6 is a detailed block diagram of one embodiment of a Chireix amplifier subsystem;

Please replace paragraph [0050] with the following paragraph:

~~FIG. 8~~ FIG. 7 is a block diagram of a signal processing system according to another embodiment of the invention; and

Please replace paragraph [0051] with the following paragraph:

~~FIG. 9~~ FIG. 8 is a detailed block diagram of a system incorporating the feature shown in FIGS. 3, 4 and 7. ~~3, 4 and 8.~~

Please replace paragraph [0160] with the following paragraph:

~~Referring to FIG. 6, a circuit for implementing the magnitude adjustment is illustrated. As can be seen, the magnitude 400~~ That is, the magnitude of the portion of the system output signal is multiplied with the factor A.sub.sx(k) by way of a multiplier ~~multiplier 410~~. The result is to be used in calculating the desired predistortion modification. This result is also subtracted from the magnitude (.vertline.x.sub..delta.(k).vertline.) of the delayed signal by way of an adder. ~~adder 420.~~ The result of the subtraction is multiplied by the update step size A by way of a multiplier ~~multiplier 430~~ and added to the factor A.sub.sx(k) by another adder ~~adder 440~~ to produce the next value in the sequence for the factor. The delay element ~~element 450~~ delays the resulting value until it is ready for use.

Please replace paragraph [0163] with the following paragraph:

Regarding the amplifier subsystem 10, FIG.6 ~~FIG. 7~~ illustrates one embodiment of the subsystem 10. In FIG.6 ~~FIG. 7,~~ the signal decomposer 20 of FIG. 1 comprises a phasor fragmentation engine 20A along with phase modulation units 60A, 60B. The fragmentation

engine 20A receives the magnitude (M) and phase (.phi.) representing the predistorted signal. The phasor fragmentation engine 20A deconstructs a predetermined modulation waveform (the predistorted signal) into signal components which are of equal and constant magnitude. Further information regarding the phasor fragmentation engines may be found in the applicant's co-pending application U.S. application Ser. No. 10/205,743 entitled COMPUTATIONAL CIRCUITS AND METHODS FOR PROCESSING MODULATED SIGNALS HAVING NON-CONSTANT ENVELOPES, which is hereby incorporated by reference. In FIG.6 ~~FIG. 7,~~ these signal components are denoted by angles .alpha. and .beta.. These components are each received by RF modulation and filtering blocks 60A, 60B which process the components to produce RF modulated and filtered versions of the components. The signal component 70A is an RF signal with phase .alpha. while signal component 70B is an RF signal with phase .delta.. These components 70A, 70B are then amplified by amplifiers 90A, 90B. The amplified components are then recombined using combiner 100. It should be noted that the phase modulation, also known as carrier modulation, may also introduce some undesired amplitude modulation. Signal decomposition methods other than the phasor fragmentation referred to above may also be used by the signal decomposer 20.

Please replace paragraph [0165] with the following paragraph:

It should further be noted that while those are only two parallel amplifiers 90A, 90B in FIG. 1 and FIG. 6, ~~FIG. 7,~~ multiple parallel amplifiers may be used as long as the decomposer 20 decomposes the predistorted signal 130 into enough components so that each component is separately amplified and phase modulated in parallel with the other components.

Please replace paragraphs [0168] and [0169] with the following two paragraphs:

While the above embodiment amplifies the input signal, albeit separately for each component, this need not be the only signal processing accomplished after the input signal is decomposed. Referring to ~~FIG. 8,~~FIG. 7 such a generalized system (which may be part of a larger signal transmission system) is illustrated. The predistortion subsystem 120 predistorts an incoming signal 30 and compensates for distortions introduced in the system output signal 110 by the improper or imperfect recombining of the input signals components. These components are produced by the signal decomposer 20 and are separately processed by signal component

processor blocks 75A, 75B. The processing executed by the blocks 75A, 75B may take the form of amplification (as in the embodiment above), phase modulation, a combination of the two, or any other signal processing which may be desired. As an example, each of the signal components illustrated in ~~FIG. 7~~FIG. 6 may be separately phase modulated in addition to being amplified by amplifiers 90A-90B. The phase modulation may be accomplished separately or be incorporated in the signal decomposer or, as contemplated for the implementation illustrated in ~~FIG. 7~~FIG. 6, incorporated into the modulation and filtering blocks 60A, 60B.

As can be seen in ~~FIG. 8,~~FIG. 7 the signal processing subsystem 10A receives the predistored signal from the predistortion subsystem 120. After being received, the predistorted signal is decomposed by the signal decomposer 20 into components. These components are then separately processed by the signal component processor blocks 75A, 75B and are then recombined by the recombiner 100.

Please replace paragraphs [0172] and [0173] with the following two paragraphs:

Referring to ~~FIG. 9,~~ FIG. 8, a detailed block diagram of a system incorporating the features illustrated in FIGS. ~~3, 4 and 8~~ 3, 4 and 7 is presented. As can be seen, the adaptive predistortion block 120 in ~~FIG. 8,~~FIG. 7 is comprised of the separate magnitude delay 240 and phase delay 270 along with a magnitude predistortion calculation block 260A. The inputs of these calculation blocks 230A, 260A are the delayed input signals from the delay blocks 240, 270 and the adjusted feedback signals from the magnitude adjustment blocks 410 and the phase adjustment block 420. After the magnitude and phase predistortion modification are, calculated, then the magnitude LUT block 220A and the phase LUT block 250A apply the predistortions. It should be noted that the magnitude LUT block 220A includes the magnitude LUT 220 and the magnitude LUT update block 230 shown in FIG. 3. Similarly, the phase LUT block 250A incorporates the phase LUT 250 and the phase LUT update block 260 illustrated in FIG. 3.

As can also be seen, the feedback signal processing block 400 illustrated in ~~FIG. 8,~~FIG. 7 is comprised of the Cartesian to polar coordinate conversion block 340 which feeds the magnitude adjustment block 410 and the phase adjustment block 420.